EAST SEARCH

5/15/04

L#	Hits	Search String	Databases
L1	1593	dynamic and (power adj dissipation) and ((integrated adj circuit) or ic) and (simulat$6 or model$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	100	1 and (dynamic near10 (power adj dissipation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	22	2 and (annotat$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L2:

US RE31545 E	Feed-forward amplifier	19840327	330/149
US 6735683 B2	Single-chip microcomputer with hierarchical internal bus structure having data and address signal lines coupling CPU with other processing elements	20040511	712/1
US 6728941 B2	Method of modeling the crossover current component in submicron CMOS integrated circuits designs	20040427	716/5
US 6717461 B2	Circuits with dynamic biasing	20040406	327/552
US 6683492 B2	Circuits with dynamic biasing	20040127	327/552
US 6642543 B1	Thin and thick gate oxide transistors on a functional block of a CMOS circuit residing within the core of an IC chip	20031104	257/72
US 6605806 B2	System and method for generating signals representing infrared radiation	20030812	250/332
US 6592764 B1	Block copolymer processing for mesostructured inorganic oxide materials	20030715	210/660
US 6591294 B2	Processing system with microcomputers each operable in master and slave modes using configurable bus access control terminals and bus use priority signals	20030708	709/209
US 6578176 B1	Method and system for genetic algorithm based power optimization for integrated circuit designs	20030610	716/2
US 6559681 B1	Resonant logic and the implementation of low power digital integrated circuits	20030506	326/98
US 6542846 B1	Thermal management system for a portable ultrasound imaging device	20030401	702/132
US 6529861 B1	Power consumption reduction for domino circuits	20030304	703/14
US 6513137 B1	Test method and apparatus using energy consumption ratio	20030128	714/736
US 6493863 B1	Method of designing semiconductor integrated circuit	20021210	716/18
US 6448816 B1	Resonant logic and the implementation of low power digital integrated circuits	20020910	326/98
US 6417705 B1	Output driver with DLL control of output driver strength	20020709	327/158
US 6415181 B1	Implantable medical device incorporating adiabatic clock-powered logic	20020702	607/16
US 6397170 B1	Simulation based power optimization	20020528	703/14
US 6396137 B1	Integrated voltage/current/power regulator/switch system and method	20020528	257/691
US 6389507 B1	Memory device search system and method	20020514	711/108

US 6373340 B1	High-efficiency audio power amplifier	20020416	330/297
US 6366061 B1	Multiple power supply circuit architecture	20020402	323/223
US 6346427 B1	Parameter adjustment in a MOS integrated circuit	20020212	438/10
US 6345379 B1	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	20020205	716/4
US 6333656 B1	Flip-flops	20011225	327/202
US 6324678 B1	Method and system for creating and validating low level description of electronic design	20011127	716/18
US 6304130 B1	Bias circuit for depletion mode field-effect transistors	20011016	327/430
US 6297668 B1	Serial device compaction for improving integrated circuit layouts	20011002	326/101
US 6285247 B1	Optimized low voltage CMOS operation	20010904	327/544
US 6252448 B1	Coincident complementary clock generator for logic circuits	20010626	327/259
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic device	20010410	716/1
US 6212665 B1	Efficient power analysis method for logic cells with many output switchings	20010403	716/4
US 6198324 B1	Flip flops	20010306	327/202
US 6181123 B1	Digital programmable direct current to direct current (DC-DC) voltage-down converter	20010130	323/351
US 6163174 A	Digital buffer circuits	20001219	326/108
US 6157903 A	Method of minimizing macrocell characterization time for state dependent power analysis	20001205	703/14
US 6100716 A	Voltage excursion detection apparatus	20000808	326/68
US 6087886 A	Hybrid dual threshold transistor multiplexer	20000711	327/408
US 6075932 A	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	20000613	716/4
US 5982309 A	Parallel-to-serial CMOS data converter with a selectable bit width mode D flip-flop M matrix	19991109	341/101
US 5982211 A	Hybrid dual threshold transistor registers	19991109	327/202
US 5870308 A	Method and system for creating and validating low-level description of electronic design	19990209	716/18
US 5862460 A	Power control circuit for a radio frequency transmitter	19990119	455/116
US 5838947 A	Modeling, characterization and simulation of integrated circuit power behavior	19981117	703/14
US 5818261 A	Pseudo differential bus driver/receiver for field programmable devices	19981006	326/86
US 5801958 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	19980901	716/18
US 5796624 A	Method and apparatus for designing circuits for wave pipelining	19980818	703/14
US 5787011 A	Low-power design techniques for high-performance CMOS circuits	19980728	716/2
US 5740407 A	Method of generating power vectors for circuit power dissipation simulation having both combinational and sequential logic circuits	19980414	703/13

US 5701094 A	Logic circuits for wave pipelining	19971223	326/113
US 5696694 A	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	19971209	716/5
US 5692160 A	Temperature, process and voltage variant slew rate based power usage simulation and method	19971125	703/23
US 5682320 A	Method for electronic memory management during estimation of average power consumption of an electronic circuit	19971028	716/4
US 5673420 A	Method of generating power vectors for cell power dissipation simulation	19970930	716/4
US 5668732 A	Method for estimating power consumption of a cyclic sequential electronic circuit	19970916	702/60
US 5663638 A	Calorimetric RF power meter with dynamic zeroing and constant temperature and power dissipation in the calorimetric bridge	19970902	324/95
US 5640115 A	Self-enabling latch	19970617	327/219
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5612636 A	Short circuit power optimization for CMOS circuits	19970318	326/83
US 5598344 A	Method and system for creating, validating, and scaling structural description of electronic device	19970128	716/18
US 5587682 A	Four-quadrant biCMOS analog multiplier	19961224	327/357
US 5581563 A	Design for testability technique of CMOS and BICMOS ICS	19961203	714/724
US 5572436 A	Method and system for creating and validating low level description of electronic design	19961105	716/18
US 5557531 A	Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation	19960917	716/1
US 5555201 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	19960910	716/1
US 5553002 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface	19960903	716/11
US 5544066 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints	19960806	716/18
US 5541849 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters	19960730	716/18
US 5528177 A	Complementary field-effect transistor logic circuits for wave pipelining	19960618	326/113
US 5521834 A	Method and apparatus for calculating dynamic power dissipation in CMOS integrated circuits	19960528	716/6
US 5426603 A	Dynamic RAM and information processing system using the same	19950620	365/149

US 5416861 A	Optical synchronous clock distribution network and high-speed signal distribution network	19950516	385/14
US 5321639 A	Dual-scale topology optoelectronic matrix algebraic processing system	19940614	708/7
US 5311083 A	Very low voltage inter-chip CMOS logic signaling for large numbers of high-speed output lines each associated with large capacitive loads	19940510	326/68
US 5258713 A	Impedance generator for a telephone line interface circuit	19931102	326/62
US 5021988 A	Semiconductor neural network and method of driving the same	19910604	706/39
US 4752750 A	Hybrid programmable transversal filter	19880621	333/166
US 4633425 A	Switched capacitor filter utilizing a differential input and output circuit	19861230	708/819
US 4633223 A	DC offset correction circuit utilizing switched capacitor differential integrator	19861230	341/118
US 4599573 A	Switched capacitor filter utilizing a differential input and output circuit and method	19860708	330/107
US 4574250 A	Switched capacitor filter utilizing a differential input and output circuit and method	19860304	330/258
US 4567386 A	Integrated logic circuit incorporating fast sample control	19860128	326/97
US 4460985 A	Sense amplifier for MOS static memory array	19840717	365/207
US 4405899 A	High pass filter and method of making same	19830920	330/107
US 4146844 A	Feed-forward amplifier	19790327	330/149
US 3866176 A	Address selection circuit for storage arrays	19750211	340/14.4
US 20030233527 A1	Single-chip microcomputer	20031218	712/1
US 20030217297 A1	Method and apparatus for software-assisted thermal management for electronic systems	20031120	713/300
US 20030210101 A1	MEMS-based, computer systems, clock generation and oscillator circuits and LC-tank apparatus for use therein	20031113	331/117FE
US 20030177460 A1	Method of modeling the crossover current component in submicron CMOS integrated circuits designs	20030918	716/5
US 20030145241 A1	Method and apparatus for reducing leakage power in a cache memory using adaptive time-based decay	20030731	713/320
US 20030076154 A1	Controlling circuit power consumption through supply voltage control	20030424	327/534
US 20030070013 A1	Method and apparatus for reducing power consumption in a digital processor	20030410	710/59
US 20030046514 A1	Single-chip microcomputer	20030306	712/33
US 20020175390 A1	Electronic circuit device, system, and method	20021128	257/481
US 20020163359 A1	Data transformation for the reduction of power and noise in CMOS structures	20021107	326/81
US 20020133668 A1	Memory device search system and method	20020919	711/108
US 20020049918 A1	Method and apparatus for reducing leakage power in a cache memory	20020425	713/300
US 20020007430 A1	Single-chip microcomputer	20020117	710/110

IEEE Xplore® RELEASE 1.7

1) Enter a single keyword, phrase, or Boolean expression.
Example: acoustic imaging (means the phrase acoustic imaging plus any stem variations)
2) Limit your search by using search operators and field codes, if desired.
Example: optical <and> (fiber <or> fibre) <in> ti
3) Limit the results by selecting Search Options.
4) Click Search. See Search Examples

```
dynamic and "power dissipation" and
("integrated circuit*" or ic) and
(simulat* or model*)
```

Start Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search operators: <and> <or> <not> <in> More

Field codes: au (author), ti (title), ab (abstract), jn (publication name), de (index term) More

Search Options:

Select publication types:

- [x] IEEE Journals
- [x] IEE Journals
- [x] IEEE Conference proceedings
- [x] IEE Conference proceedings
- [x] IEEE Standards

Select years to search:

From year: All to Present

Organize search results by:

Sort by: Year

In: Ascending order

List 50 Results per page

Your search matched **120** of **991126** documents.

A maximum of **120** results are displayed, **50** to a page, sorted by **publication year** in **ascending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

dynamic and Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Injection-coupled memory: A high-density static bipolar memory**
Wiedmann, S.K.;
Solid-State Circuits, IEEE Journal of , Volume: 8 Issue: 5 , Oct 1973
Page(s): 332 -337

[Abstract] [PDF Full-Text (1064 KB)] **IEEE JNL**

2 **Model and performance of hot-electron MOS transistors for VLSI**
Hoefflinger, B.; Sibbert, H.; Zimmer, G.;
Solid-State Circuits, IEEE Journal of , Volume: 14 Issue: 2 , Apr 1979
Page(s): 435 -442

[Abstract] [PDF Full-Text (1120 KB)] **IEEE JNL**

3 **Reliability Evaluation of Aluminum-Metallized MOS Dynamic RAM's in Plastic Packages in High Humidity and Temperature Environments**
Striny, K.; Schelling, A.;
Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [see also IEEE Trans. on Components, Packaging, and Manufacturing Technology, Part A, B, C] , Volume: 4 Issue: 4 , Dec 1981
Page(s): 476 -481

[Abstract] [PDF Full-Text (832 KB)] **IEEE JNL**

4 **SOS/CMOS as a High-Performance LSI Device**
Okuto, Y.; Fukuma, M.; Ohno, Y.;
Solid-State Circuits, IEEE Journal of , Volume: 17 Issue: 2 , Apr 1982
Page(s): 204 -207

[Abstract] [PDF Full-Text (744 KB)] **IEEE JNL**

5 **Performance Limits of CMOS ULSI**
Pfiester, J.R.; Shott, J.D.; Meindl, J.D.;
Solid-State Circuits, IEEE Journal of , Volume: 20 Issue: 1 , Feb 1985
Page(s): 253 -263

[Abstract] [PDF Full-Text (1768 KB)] **IEEE JNL**

6 **A comparison of CMOS circuit techniques: differential cascode voltage switch logic versus conventional logic**
Chu, K.M.; Pulfrey, D.L.;
Solid-State Circuits, IEEE Journal of , Volume: 22 Issue: 4 , Aug 1987
Page(s): 528 -532

[Abstract] [PDF Full-Text (592 KB)] **IEEE JNL**

7 **A 9.5 GHz commercially available 1/4 GaAs dynamic prescaler with suppressed noise performance**
Takahashi, M.; Itoh, H.; Ueda, K.; Yamamoto, R.;
Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1988. Digest of Papers., IEEE 1988 , 24-25 May 1988
Page(s): 31 -35

[Abstract] [PDF Full-Text (380 KB)] **IEEE CNF**

8 **Switch-driver circuit suitable for high-order switched-capacitor filters implemented in GaAs**
Harrold, S.J.;
Electronics Letters , Volume: 24 Issue: 15 , 21 July 1988
Page(s): 982 -984

[Abstract] [PDF Full-Text (160 KB)] **IEE JNL**

9 **A 9.5 GHz commercially available 1/4 GaAs dynamic prescaler**
Takahashi, M.; Itoh, H.; Ueda, K.; Yamamoto, R.;
Microwave Theory and Techniques, IEEE Transactions on , Volume: 36 Issue: 12 , Dec 1988
Page(s): 1913 -1919

[Abstract] [PDF Full-Text (648 KB)] **IEEE JNL**

10 **Theoretical evaluation of a novel design for digital GaAs ICs**
Passlack, M.; Elschner, H.; Stenzel, R.;
Solid-State Circuits, IEEE Journal of , Volume: 23 Issue: 5 , Oct. 1988
Page(s): 1249 -1256

[Abstract] [PDF Full-Text (536 KB)] **IEEE JNL**

---

11 **RIPAC: a VLSI processor for speech recognition**
Licciardi, L.; Paolini, M.; Tasso, R.; Torielli, A.; Cecinati, R.;
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989 , 15-18 May 1989
Page(s): 20.6/1 -20.6/4

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

---

12 **Power dissipation estimate by switch level simulation [CMOS circuits]**
Tjarnstrom, R.;
Circuits and Systems, 1989., IEEE International Symposium on , 8-11 May 1989
Page(s): 881 -884 vol.2

[Abstract] [PDF Full-Text (244 KB)] **IEEE CNF**

---

13 **Electrically modifiable nonvolatile synapses for neural networks**
White, M.H.; Chen, C.-Y.;
Circuits and Systems, 1989., IEEE International Symposium on , 8-11 May 1989
Page(s): 1213 -1216 vol.2

[Abstract] [PDF Full-Text (280 KB)] **IEEE CNF**

---

14 **Estimation of power dissipation in CMOS combinational circuits**
Devadas, S.; Keutzer, K.; White, J.;
Custom Integrated Circuits Conference, 1990., Proceedings of the IEEE 1990 , 13-16 May 1990
Page(s): 19.7/1 -19.7/6

[Abstract] [PDF Full-Text (580 KB)] **IEEE CNF**

---

15 **Optimization of high-speed CMOS logic circuits with analytical models for signal delay, chip area, and dynamic power dissipation**
Hoppe, B.; Neuendorf, G.; Schmitt-Landsiedel, D.; Specks, W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 9 Issue: 3 , March 1990
Page(s): 236 -247

[Abstract] [PDF Full-Text (992 KB)] **IEEE JNL**

---

16 **Temporal models for neural nets for integrated circuit implementations**
Salam, F.M.A.;
Circuits and Systems, 1991., IEEE International Sympoisum on , 11-14 June 1991
Page(s): 1456 vol.3

[Abstract] [PDF Full-Text (92 KB)] **IEEE CNF**

---

17 **Power calculation for high density CMOS gate arrays**
Eisenmann, W.; Kohl, M.;
Euro ASIC '91 , 27-31 May 1991
Page(s): 198 -203

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

---

18 **An experimental 1.5-V 64-Mb DRAM**
Nakagome, Y.; Tanaka, H.; Takeuchi, K.; Kume, E.; Watanabe, Y.; Kaga, T.; Kawamoto, Y.; Murai, F.; Izawa, R.; Hisamoto, D.; Kisu, T.; Nishida, T.; Takeda, E.; Itoh, K.;
Solid-State Circuits, IEEE Journal of , Volume: 26 Issue: 4 , April 1991
Page(s): 465 -472

[Abstract] [PDF Full-Text (808 KB)] **IEEE JNL**

---

19 **Analog operation in CMOS latch circuit for reducing dynamic power dissipation**
Dejhan, K.; Cheevasuvit, F.; Tipsuwanporn, V.; Trisuwannawat, T.; Prommas, E.;
Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on , 9-12 Aug. 1992
Page(s): 544 -547 vol.1

[Abstract] [PDF Full-Text (284 KB)] **IEEE CNF**

---

20 **Optimizing adders for WSI**
Callaway, T.K.; Swartzlander, E.E., Jr.;
Wafer Scale Integration, 1992. Proceedings., [4th] International Conference on , 22-24 Jan. 1992
Page(s): 251 -260

[Abstract] [PDF Full-Text (308 KB)] **IEEE CNF**

---

21 **A 288-kb fully parallel content addressable memory using a stacked-capacitor cell structure**
Yamagata, T.; Mihara, M.; Hamamoto, T.; Murai, Y.; Kobayashi, T.; Yamada, M.; Ozaki, H.;
Solid-State Circuits, IEEE Journal of , Volume: 27 Issue: 12 , Dec. 1992
Page(s): 1927 -1933

[Abstract] [PDF Full-Text (780 KB)] **IEEE JNL**

---

22 **Estimation of power dissipation in CMOS combinational circuits using Boolean function manipulation**
Devadas, S.; Keutzer, K.; White, J.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 11 Issue: 3 , March 1992
Page(s): 373 -383

[Abstract] [PDF Full-Text (916 KB)] **IEEE JNL**

---

23 **A 3V-125 MHz CMOS continuous-time filter**
Zele, R.H.; Lee, S.-S.; Allstot, D.J.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , 3-6 May 1993
Page(s): 1164 -1167 vol.2

[Abstract] [PDF Full-Text (224 KB)] **IEEE CNF**

---

24 **Design and evaluation of a current-mode multiple-valued PLA based on a resonant tunnelling transistor model**
Deng, X.; Hanyu, T.; Kameyama, M.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 141 Issue: 6 , Dec. 1994
Page(s): 445 -450

[Abstract] [PDF Full-Text (328 KB)] **IEE JNL**

---

25 **Electrical packaging requirements for low-voltage ICs-3.3 V high-performance CMOS devices as a case study**
Senthinathan, R.; Mehra, A.; Mahalingam, M.; Doi, Y.; Astrain, H.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 17 Issue: 4 , Nov. 1994
Page(s): 493 -504

[Abstract] [PDF Full-Text (1064 KB)] **IEEE JNL**

---

26 **Design of CMOS tapered buffer for minimum power-delay product**
Jso-Sun Choi; Kwyro Lee;
Solid-State Circuits, IEEE Journal of , Volume: 29 Issue: 9 , Sept. 1994
Page(s): 1142 -1145

[Abstract] [PDF Full-Text (308 KB)] **IEEE JNL**

---

27 **Channel width tapering of serially connected MOSFET's with emphasis on power dissipation**
Cherkauer, B.S.; Friedman, E.G.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 2 Issue: 1 , March 1994
Page(s): 100 -114

[Abstract] [PDF Full-Text (1032 KB)] **IEEE JNL**

28 **Minimizing power dissipation in non-zero skew-based clock distribution networks**
Neves, J.L.; Friedman, E.G.;
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , Volume: 3 , 28 April-3 May 1995
Page(s): 1576 -1579 vol.3

[Abstract] [PDF Full-Text (484 KB)] **IEEE CNF**

29 **Low-power high-speed continuous-time Σ-Δ modulators**
Mittal, R.; Allstot, D.J.;
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , Volume: 1 , 28 April-3 May 1995
Page(s): 183 -186 vol.1

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

30 **Vertical signal transmission in three-dimensional integrated circuits by capacitive coupling**
Kuhn, S.A.; Kleiner, M.B.; Thewes, R.; Weber, W.;
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , Volume: 1 , 28 April-3 May 1995
Page(s): 37 -40 vol.1

[Abstract] [PDF Full-Text (452 KB)] **IEEE CNF**

31 **A design framework for low power analog filter banks**
Furth, P.M.; Andreou, A.G.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , Volume: 42 Issue: 11 , Nov. 1995
Page(s): 966 -971

[Abstract] [PDF Full-Text (612 KB)] **IEEE JNL**

32 **Power consumption of static and dynamic CMOS circuits: a comparative study**
Macii, E.; Poncino, M.;
ASIC, 1996. 2nd International Conference on , 21-24 Oct. 1996
Page(s): 425 -427

[Abstract] [PDF Full-Text (236 KB)] **IEEE CNF**

33 **DC-current-free low-power A/D converter circuitry using dynamic latch comparators with divided-capacitance voltage reference**
Kotani, K.; Shibata, T.; Ohmi, T.;

Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium on , Volume: 4 , 12-15 May 1996
Page(s): 205 -208 vol.4

[Abstract] [PDF Full-Text (504 KB)] **IEEE CNF**

---

34 **Transient thermal management in electronic packaging using dynamic control of power dissipation and heat transfer**
Cao, L.; Krusius, J.P.; Korhonen, M.; Fisher, T.;
Electronic Components and Technology Conference, 1996. Proceedings., 46th , 28-31 May 1996
Page(s): 205 -211

[Abstract] [PDF Full-Text (700 KB)] **IEEE CNF**

---

35 **Optimal low power interconnect networks**
Davis, J.A.; De, V.; Meindl, J.;
VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-13 June 1996
Page(s): 78 -79

[Abstract] [PDF Full-Text (148 KB)] **IEEE CNF**

---

36 **Power dissipation analysis and optimization of deep submicron CMOS digital circuits**
Gu, R.X.; Elmasry, M.I.;
Solid-State Circuits, IEEE Journal of , Volume: 31 Issue: 5 , May 1996
Page(s): 707 -713

[Abstract] [PDF Full-Text (560 KB)] **IEEE JNL**

---

37 **Reducing power dissipation in CMOS circuits by signal probability based transistor reordering**
Hossain, R.; Zheng, M.; Albicki, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 Issue: 3 , March 1996
Page(s): 361 -368

[Abstract] [PDF Full-Text (820 KB)] **IEEE JNL**

---

38 **Optimal wire sizing and buffer insertion for low power and a generalized delay model**
Lillis, J.; Chung-Kuan Cheng; Lin, T.-T.Y.;
Solid-State Circuits, IEEE Journal of , Volume: 31 Issue: 3 , March 1996
Page(s): 437 -447

[Abstract] [PDF Full-Text (1096 KB)] **IEEE JNL**

39 **Power consumption in CMOS combinational logic blocks at high frequencies**
Parameswaran, S.; Hui Guo;
Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997
Page(s): 195 -200

[Abstract] [PDF Full-Text (440 KB)] **IEEE CNF**

40 **A stochastic wire length distribution for gigascale integration (GSI)**
Davis, J.A.; De, V.K.; Meindl, J.D.;
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 , 5-8 May 1997
Page(s): 145 -150

[Abstract] [PDF Full-Text (464 KB)] **IEEE CNF**

41 **A 50 MHz high-Q bandpass CMOS filter**
Manetakis, K.; Toumazou, C.;
Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on , Volume: 1 , 9-12 June 1997
Page(s): 309 -312 vol.1

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

42 **A 1 mV resolution 10 MS/s rail-to-rail comparator in 0.5 µm low-voltage CMOS digital process**
Rivoir, R.; Maloberti, F.;
Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on , Volume: 1 , 9-12 June 1997
Page(s): 461 -464 vol.1

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

43 **Repeater insertion to reduce delay and power in RC tree structures**
Adler, V.; Friedman, E.G.;
Signals, Systems & Computers, 1997. Conference Record of the Thirty-First Asilomar Conference on , Volume: 1 , 2-5 Nov. 1997
Page(s): 749 -752 vol.1

[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

44 **On the power dissipation in dynamic threshold silicon-on-insulator CMOS inverter**
Wei Jin; Chan, P.C.H.; Chan, M.;
Low Power Electronics and Design, 1997. Proceedings., 1997 International Symposium on , 18-20 Aug. 1997

Page(s): 247 -250

[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

---

45 **Power dissipation estimation and advantages of low operating voltages**
Packer, L.K.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Page(s): 234 -239

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

---

46 **CMOS adaptive biasing circuits for low-power applications**
Cardarilli, G.; Ferri, G.;
Microelectronics, 1997. Proceedings., 1997 21st International Conference on , Volume: 2 , 14-17 Sept. 1997
Page(s): 747 -750 vol.2

[Abstract] [PDF Full-Text (260 KB)] **IEEE CNF**

---

47 **Thermal limits of flip chip package-experimentally validated, CFD supported case studies**
Tien-Yu Tom Lee; Mahalingam, M.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 20 Issue: 1 , Feb. 1997
Page(s): 94 -103

[Abstract] [PDF Full-Text (252 KB)] **IEEE JNL**

---

48 **Low-voltage dynamic BiCMOS CLA circuit with carry skip using novel full-swing logic**
Hasan, S.M.R.; Rajagopal, C.D.;
Solid-State Circuits, IEEE Journal of , Volume: 32 Issue: 1 , Jan. 1997
Page(s): 70 -78

[Abstract] [PDF Full-Text (1612 KB)] **IEEE JNL**

---

49 **An analysis of the performance of a new high-speed single-way analog switch**
Wang Ping; Shi Yin; Li Shizu;
Solid-State and Integrated Circuit Technology, 1998. Proceedings. 1998 5th International Conference on , 21-23 Oct. 1998
Page(s): 409 -412

[Abstract] [PDF Full-Text (156 KB)] **IEEE CNF**

50 **On short circuit power estimation of CMOS inverters**
Wang, Q.; Vrudhula, S.B.K.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on , 5-7 Oct. 1998
Page(s): 70 -75

[Abstract] [PDF Full-Text (192 KB)] **IEEE CNF**

1 2 3 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **120** of **991126** documents.

A maximum of **120** results are displayed, **50** to a page, sorted by **publication year** in **ascending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

dynamic and Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

51 **A 50 Mhz 5TH order elliptic LP-filter using current mode Gm-C topology**
Kosunen, M.; Koli, K.; Halonen, K.;
Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 1 , 31 May-3 June 1998
Page(s): 512 -515 vol.1

[Abstract] [PDF Full-Text (220 KB)] **IEEE CNF**

52 **Evaluating thermal characterization accuracy using CFD codes-a package level benchmark study of IcePak™ and Flotherm®**
Zahn, B.A.;
Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM '98. The Sixth Intersociety Conference on , 27-30 May 1998
Page(s): 322 -329

[Abstract] [PDF Full-Text (796 KB)] **IEEE CNF**

53 **Circuits for low power consumption in GaAs technology**
Reina, R.; Charry, E.; Lopez, J.; Sarmiento, R.;
Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on , 30 Sept.-3 Oct. 1998
Page(s): 200 -203

[Abstract] [PDF Full-Text (72 KB)] **IEEE CNF**

54 **Cast heatsink design advantages**
Keller, K.P.;
Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM '98. The Sixth Intersociety Conference on , 27-30 May 1998
Page(s): 112 -117

[Abstract] [PDF Full-Text (460 KB)] **IEEE CNF**

55 **Power estimation of CMOS circuits via power software**
Rodnunsky, N.L.; Margala, M.; Durdle, N.G.;
Electrical and Computer Engineering, 1998. IEEE Canadian Conference on , Volume: 1 , 24-28 May 1998
Page(s): 149 -152 vol.1

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

56 **Four-quadrant analogue CMOS multiplier cell for VLSI signal and information processing**
Lau, K.T.; Lee, S.T.; Ong, V.K.S.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 145 Issue: 2 , April 1998
Page(s): 132 -134

[Abstract] [PDF Full-Text (264 KB)] **IEE JNL**

57 **Transient thermal management of portable electronics using heat storage and dynamic power dissipation control**
Lipeng Cao; Krusius, J.P.; Korhonen, M.A.; Fisher, T.S.;
Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 21 Issue: 1 , March 1998
Page(s): 113 -123

[Abstract] [PDF Full-Text (256 KB)] **IEEE JNL**

58 **Repeater design to reduce delay and power in resistive interconnect**
Adler, V.; Friedman, E.G.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , Volume: 45 Issue: 5 , May 1998
Page(s): 607 -616

[Abstract] [PDF Full-Text (292 KB)] **IEEE JNL**

59 **CMOS interface circuitry for a low-voltage micromachined tunneling accelerometer**
Chingwen Yeh; Najafi, K.;
Microelectromechanical Systems, Journal of , Volume: 7 Issue: 1 , March 1998
Page(s): 6 -15

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

60 **A stochastic wire-length distribution for gigascale integration (GSI). II. Applications to clock frequency, power dissipation, and chip size estimation**
Davis, J.A.; De, V.K.; Meindl, J.D.;
Electron Devices, IEEE Transactions on , Volume: 45 Issue: 3 , March 1998
Page(s): 590 -597

[Abstract] [PDF Full-Text (484 KB)] **IEEE JNL**

---

61 **A 30-V row/column driver for PSCT LCD using high-voltage BiMOS process**
Jing-Jou Tang; Bin-Da Liu; Jeng Ron Wu;
ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 23-25 Aug. 1999
Page(s): 376 -379

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

---

62 **A low voltage four-quadrant CMOS analogue multiplier**
Zhi-Ming Lin; Huang, C.H.;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on , Volume: 3 , 5-8 Sept. 1999
Page(s): 1333 -1335 vol.3

[Abstract] [PDF Full-Text (172 KB)] **IEEE CNF**

---

63 **Differential current amplifiers with improved dynamic range**
Chrisanthopoulos, A.; Souliotis, G.; Haritantis, I.;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on , Volume: 1 , 5-8 Sept. 1999
Page(s): 501 -504 vol.1

[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

---

64 **A CMOS continuous-time active biquad filter for gigahertz-band applications**
Chang, Y.; Choma, J., Jr.; Wills, J.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 2 , 30 May-2 June 1999
Page(s): 656 -659 vol.2

[Abstract] [PDF Full-Text (284 KB)] **IEEE CNF**

---

65 **Passive precharge and rippled power logic (PPRPL)**
Schaevitz, S.B.; Lin, C.;
Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on , 16-17 Aug. 1999
Page(s): 249 -251

[Abstract] [PDF Full-Text (196 KB)] **IEEE CNF**

66 **Stochastic modeling of a power-managed system: construction and optimization**
Qinru Qiu; Qing Wu; Pedram, M.;
Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on , 16-17 Aug. 1999
Page(s): 194 -199

[Abstract] [PDF Full-Text (472 KB)] **IEEE CNF**

67 **Low power synthesis of dual threshold voltage CMOS VLSI circuits**
Sundararajan, V.; Parhi, K.K.;
Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on , 16-17 Aug. 1999
Page(s): 139 -144

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

68 **Low voltage CMOS op-amps for a supply close to a transistor's threshold voltage**
Ramirez-Angulo, J.; Carvajal, R.G.; Tombs, J.; Torralba, A.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 2 , 30 May-2 June 1999
Page(s): 408 -411 vol.2

[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

69 **Thermal design for flip chip on board in natural convection**
Hwang, C.-B.;
Semiconductor Thermal Measurement and Management Symposium, 1999. Fifteenth Annual IEEE , 9-11 March 1999
Page(s): 125 -132

[Abstract] [PDF Full-Text (692 KB)] **IEEE CNF**

70 **Optimizing cost and thermal performance: rapid prototyping of a high pin count cavity-up enhanced plastic ball grid array (EPBGA) package**
Zahn, B.A.;
Semiconductor Thermal Measurement and Management Symposium, 1999. Fifteenth Annual IEEE , 9-11 March 1999
Page(s): 133 -141

[Abstract] [PDF Full-Text (616 KB)] **IEEE CNF**

71 **The design of CMOS gigahertz-band continuous-time active lowpass filters with Q-enhancement circuits**
Yugu Chang; Choma, J., Jr.; Wills, J.;
VLSI, 1999. Proceedings. Ninth Great Lakes Symposium on , 4-6 March 1999
Page(s): 358 -361

[Abstract] [PDF Full-Text (180 KB)] **IEEE CNF**

---

72 **Altering transistor positions: impact on the performance and power dissipation of dynamic latches and flip-flops**
Mishra, S.M.; Rofail, S.S.; Seng, Y.K.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 146 Issue: 5 , Oct. 1999
Page(s): 279 -284

[Abstract] [PDF Full-Text (352 KB)] **IEE JNL**

---

73 **Time-domain model for power dissipation of CMOS buffers driving lossy lines**
Cappuccino, G.; Cocorullo, G.;
Electronics Letters , Volume: 35 Issue: 12 , 10 Jun 1999
Page(s): 959 -960

[Abstract] [PDF Full-Text (240 KB)] **IEE JNL**

---

74 **Sequence compaction for power estimation: theory and practice**
Marculescu, R.; Marculescu, D.; Pedram, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 Issue: 7 , July 1999
Page(s): 973 -993

[Abstract] [PDF Full-Text (456 KB)] **IEEE JNL**

---

75 **A new true-single-phase-clocking BiCMOS dynamic pipelined logic family for high-speed, low-voltage pipelined system applications**
Yuh-Kuang Tseng; Chung-Yu Wu;
Solid-State Circuits, IEEE Journal of , Volume: 34 Issue: 1 , Jan. 1999
Page(s): 68 -79

[Abstract] [PDF Full-Text (328 KB)] **IEEE JNL**

---

76 **An assertion based technique for transistor level dynamic power estimation**
Savithri, S.; Venkatesan, R.; Bhaskar, S.;
VLSI Design, 2000. Thirteenth International Conference on , 3-7 Jan. 2000
Page(s): 34 -37

[Abstract] [PDF Full-Text (52 KB)] **IEEE CNF**

---

77 **Data-driven dynamic logic versus NP-CMOS logic, a comparison**
Rafati, R.; Charaki, A.Z.; Fakhraie, S.M.; Smith, K.C.;
Microelectronics, 2000. ICM 2000. Proceedings of the 12th International Conference on , 31 Oct.-2 Nov. 2000
Page(s): 57 -60

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

---

78 **Power optimization of delay constrained circuits**
Nayak, A.; Haldar, M.; Banerjee, P.; Chunhong Chen; Sarrafzadeh, M.;
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International , 13-16 Sept. 2000
Page(s): 305 -309

[Abstract] [PDF Full-Text (604 KB)] **IEEE CNF**

---

79 **A self-biased low voltage, low power, CMOS transconductor stage**
Fedeli, M.; Vacchi, C.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 5 , 28-31 May 2000
Page(s): 649 -652 vol.5

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

---

80 **A 1-V low power rail-to-rail analog CMOS multi-function filter with configurable capability**
Yu-Cherng Hung; Bin-Da Liu;
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on , 28-30 Aug. 2000
Page(s): 115 -118

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

---

81 **Low-power sensing and digitization of cardiac signals based on sigma-delta conversion**
Gerosa, A.; Novo, A.; Neviani, A.;
Low Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on , 26-27 July 2000
Page(s): 216 -218

[Abstract] [PDF Full-Text (276 KB)] **IEEE CNF**

---

82 **Modeling of short circuit power consumption using timing-only logic cell macromodels**
da Costa, E.A.C.; Cortes, F.P.; Cardoso, R.; Carro, L.; Bampi, S.;
Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on

, 18-24 Sept. 2000
Page(s): 222 -227

[Abstract] [PDF Full-Text (432 KB)] **IEEE CNF**

---

83 **Limits to voltage scaling from the low power perspective**
Forestier, A.; Stan, M.R.;
Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on , 18-24 Sept. 2000
Page(s): 365 -370

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

---

84 **Power minimization by simultaneous dual-V_{th} assignment and gate-sizing**
Liqiong Wei; Kaushik Roy; Cheng-Kok Koh;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Page(s): 413 -416

[Abstract] [PDF Full-Text (388 KB)] **IEEE CNF**

---

85 **Wafer level burn-in**
Conti, D.R.; Van Horn, J.;
Electronic Components and Technology Conference, 2000. 2000 Proceedings. 50th , 21-24 May 2000
Page(s): 815 -821

[Abstract] [PDF Full-Text (512 KB)] **IEEE CNF**

---

86 **Dynamic back bias CMOS driver for low-voltage applications**
Moisiadis, Y.; Bouras, I.; Arapoyanni, A.;
Electronics Letters , Volume: 36 Issue: 2 , 20 Jan. 2000
Page(s): 135 -136

[Abstract] [PDF Full-Text (100 KB)] **IEE JNL**

---

87 **Dynamic power of CMOS gates driving lossy transmission lines**
Cappuccino, G.; Corsonello, P.; Cocorullo, G.; Perri, S.; Staino, G.;
Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on , Volume: 3 , 2-5 Sept. 2001
Page(s): 1579 -1582 vol.3

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

---

88 **A "divide and conquer" technique for the design of wide dynamic range continuous time filters**
Palaskas, G.; Tsividis, Y.;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 1 , 6-9 May 2001
Page(s): 252 -255 vol. 1

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

---

89 **A CMOS differential logic for low-power and high-speed applications**
Moisiadis, Y.; Bouras, I.; Arapoyanni, A.;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 4 , 6-9 May 2001
Page(s): 140 -143 vol. 4

[Abstract] [PDF Full-Text (292 KB)] **IEEE CNF**

---

90 **A switched-current sample and hold circuit for low frequency applications**
de Lira Mendes, E.; Loumeau, P.; Naviner, J.-F.;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 1 , 6-9 May 2001
Page(s): 452 -455 vol. 1

[Abstract] [PDF Full-Text (260 KB)] **IEEE CNF**

---

91 **Crosstalk fault detection by dynamic I_{dd}**
Xiaoyun Sun; Seonki Kim; Vinnakota, B.;
Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference on , 4-8 Nov. 2001
Page(s): 375 -378

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

---

92 **A two-phase, four and five boosting ratio, charge pump cell for LCD driver**
Hairong Yu; Zhiliang Chen;
ASIC, 2001. Proceedings. 4th International Conference on , 23-25 Oct. 2001
Page(s): 266 -270

[Abstract] [PDF Full-Text (387 KB)] **IEEE CNF**

---

93 **Spiking analog neuron circuit design, analysis, and simulation**
Fujii, R.H.; Nemoto, R.; Satou, N.;
Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on , Volume: 1 , 14-17 Aug. 2001
Page(s): 482 -486 vol.1

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

---

94 **A low-power digital signal processor core by minimizing inter-data switching activities**
Yi-Wen Wu; Chen, O.T.-C.; Ruey-Liang Ma;
Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on , Volume: 1 , 14-17 Aug. 2001
Page(s): 172 -175 vol.1

[Abstract] [PDF Full-Text (373 KB)] **IEEE CNF**

---

95 **ESD protection under grounded-up bond pads in 0.13 µm eight-level copper metal, fluorinated silicate glass low-k intermetal dielectric CMOS process technology**
Kuo-Yu Chou; Ming-Jer Chen;
Electron Device Letters, IEEE , Volume: 22 Issue: 7 , July 2001
Page(s): 342 -344

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

---

96 **Stochastic modeling of a power-managed system-construction and optimization**
Qiu, Q.; Qu, Q.; Pedram, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 Issue: 10 , Oct. 2001
Page(s): 1200 -1217

[Abstract] [PDF Full-Text (360 KB)] **IEEE JNL**

---

97 **An optimal variable voltage scheduling**
Huang, S.; Chen, C.; Ahmadi, M.; Mokrian, P.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 1 , 4-7 Aug. 2002
Page(s): I -479-82 vol.1

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

---

98 **Class AB VHF CMOS active inductor**
Thanachayanont, A.; Sae Ngow, S.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 1 , 4-7 Aug. 2002
Page(s): I -64-7 vol.1

[Abstract] [PDF Full-Text (290 KB)] **IEEE CNF**

---

99 **Variable threshold voltage keeper for contention reduction in dynamic circuits**
Kursun, V.; Friedman, E.G.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 2002
Page(s): 314 -318

[Abstract] [PDF Full-Text (419 KB)] **IEEE CNF**

100 **An oldest-first selection logic implementation for non-compacting issue queues [microprocessor power reduction]**
Buyuktosunoglu, A.; El-Moursy, A.; Albonesi, D.H.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 2002
Page(s): 31 -35

[Abstract] [PDF Full-Text (454 KB)] **IEEE CNF**

[Prev] 1 2 3 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Terms used **dynamic** and **power dissipation** and **integrated circuit** or **ic** and **simulat** or **model**

Found **4,333** of **132,857**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

2 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

3 IC test using the energy consumption ratio

Wanli Jiang, Bapiraju Vinnakota

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation conference**

Full text available: pdf(89.67 KB) Additional Information: full citation, references, citings, index terms

4 Keynote speech 1: Elements of low power design for integrated systems

Sung-Mo Kang

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(281.58 KB) Additional Information: full citation, abstract, references, index terms

The increasing prominence of portable systems and the need to limit power consumption and hence, heat dissipation in very high density VLSI chips have led to rapid and innovative developments in low power design recently. Leakage control is becoming critically important for deep sub-100nm technologies due to the scaling down of threshold voltage and gate oxide thickness of transistors. In this paper, we discuss major sources of power dissipation in VLSI systems, and various low power design tech ...

Keywords: CMOS, VLSI, low power integrated circuits

5 Power estimation techniques for integrated circuits

Farid N. Najm

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(218.32 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

With the advent of portable and high-density microelectronic devices, the power dissipation of very large scale integrated (VLSI) circuits is becoming a critical concern. Accurate and efficient power estimation during the design phase is required in order to meet the power specifications without a costly redesign process. Recently, a variety of power estimation techniques have been proposed, most of which are based on: 1) the use of simplified delay models, and 2) modeling the long-term behavior ...

Keywords: power estimation VLSI circuit survey tutorial probability statistics

6 Interconnect analysis for SoCs and microprocessors: Interconnect-power dissipation in a microprocessor

Nir Magen, Avinoam Kolodny, Uri Weiser, Nachum Shamir

February 2004 **Proceedings of the 2004 international workshop on System level interconnect prediction**

Full text available: pdf(249.61 KB) Additional Information: full citation, abstract, references, index terms

Interconnect power is dynamic power dissipation due to switching of interconnection capacitances. This paper describes the characterization of interconnect power in a state-of-the-art high-performance microprocessor designed for power efficiency. The analysis showed that interconnect power is over 50% of the dynamic power. Over 90% of the interconnect power is consumed by only 10% of the interconnections. Relations of interconnect power to wire length distribution and hierarchy level of nets wer ...

Keywords: interconnect power, low-power design, routing, wire spacing

7 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges

Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index terms

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

8 Challenges in integrated CMOS transceivers for short distance wireless

Khurram Muhammad, Robert B. Straszewski, Poras T. Balsara

March 2001 **Proceedings of the 11th Great Lakes Symposium on VLSI**

Full text available: pdf(797.97 KB) Additional Information: full citation, references, index terms

9 Low power RF integrated circuits: principles and practice
A. A. Abidi, H. Darabi
August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**
Full text available: pdf(191.14 KB) Additional Information: full citation, references, index terms

10 Iterative schedule optimization for voltage scalable distributed embedded systems
Marcus T. Schmitz, Bashir M. Al-Hashimi, Petru Eles
February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1
Full text available: pdf(273.28 KB) Additional Information: full citation, abstract, references, index terms

We present an iterative schedule optimization for multirate system specifications, mapped onto heterogeneous distributed architectures containing dynamic voltage scalable processing elements (DVS-PEs). To achieve a high degree of energy reduction, we formulate a generalized DVS problem, taking into account the power variations among the executing tasks. An efficient heuristic is presented that identifies optimized supply voltages by not only "simply" exploiting slack time, but under the addition ...

Keywords: Dynamic voltage scaling, embedded systems, energy minimization, heterogeneous distributed systems, scheduling, system synthesis

11 Architecture Analysis and Automation: Dynamic power consumption in Virtex™-II FPGA family
Li Shang, Alireza S. Kaviani, Kusuma Bathala
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(309.07 KB) Additional Information: full citation, abstract, references, citings

This paper analyzes the dynamic power consumption in the fabric of Field Programmable Gate Arrays (FPGAs) by taking advantage of both simulation and measurement. Our target device is Xilinx Virtex™-II family, which contains the most recent and largest programmable fabric. We identify important resources in the FPGA architecture and obtain their utilization, using a large set of real designs. Then, using a number of representative case studies we calculate the switching activity correspondi ...

12 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadl H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

13 Getting to the bottom of deep submicron
Dennis Sylvester, Kurt Keutzer
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.22 MB) Additional Information: full citation, references, citings, index terms

Keywords: ASIC, CMOS scaling, gate delay, interconnect modeling, power dissipation, signal integrity, wirelength

14 Future performance challenges in nanometer design
Dennis Sylvester, Himanshu Kaul
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(252.60 KB) Additional Information: full citation, abstract, references, citings, index terms

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes< 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

15 Leakage Current: Leakage current in low standby power and high performance devices: trends and challenges
Geoffrey C-F Yeap
April 2002 **Proceedings of the 2002 international symposium on Physical design**

Full text available: pdf(212.42 KB) Additional Information: full citation, abstract, references, index terms

IC technology is continuing to scale according to Moore's Law, with the overall chip circuit requirements driving the MOSFET device and process integration requirements and optimal choices. In the 2001 International Technology Roadmap for Semiconductors (ITRS) [1] the driver for the high performance logic is maximizing MOSFET intrinsic speed, while the driver for low standby power logic is minimizing MOSFET leakage current. Total leakage current of a MOSFET consists of three components: off-stat ...

Keywords: CMOS technology, gate tunneling leakage, high performance, leakage current, low standby power, off-state sub-threshold leakage, system-on-a-ship (SoC)

16 Technology decomposition and mapping targeting low power dissipation
Chi-Ying Tsui, Massoud Pedram, Alvin M. Despain
July 1993 **Proceedings of the 30th international on Design automation conference**

Full text available: pdf(657.86 KB) Additional Information: full citation, references, citings, index terms

17 Keynote speech 4: Low power RF IC design for wireless communication
Domine M.W. Leenaerts
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

In this paper, the many issues around the system and circuit design of advanced RF front ends for wireless RF applications will be discussed. After a short discussion on technology related issues, design choices linked to the different circuit/system solutions will be discussed.

Keywords: LNA, PLL, RF, VCO, low power, technology, transceivers, wireless communication

18 Wireless telecom silicon integration: analog design for radio, baseband and speech spectrum
J. Sevenhans, D. Haspeslagh, J. Wenin
January 1998 **Wireless Networks**, Volume 4 Issue 1

Full text available: pdf(324.74 KB) Additional Information: full citation, abstract, references, index terms

The application today, pushing analog design for CMOS and RF-bipolar into new frontiers is definitely the mobile radio telephony. New telecom systems like GSM, PCN, DECT, DCS, Wireless in the loop...are all developing very rapidly and will enable us very soon to organise a complete telephone network with full coverage for your car, as well as in your kitchen and on your office desk. In Europe the major telecom companies have worked together to establish one common standard for cellular mobi ...

19 What is the state of the art in commercial EDA tools for low power?
K. Keutzer, O. Coudert, R. Haddad
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**
Full text available: pdf(196.98 KB) Additional Information: full citation, references, citings, index terms

20 Tools and architectures for power minimization: Active leakage power optimization for FPGAs
Jason H. Anderson, Farid N. Najm, Tim Tuan
February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
Full text available: pdf(214.96 KB) Additional Information: full citation, abstract, references, index terms

We consider active leakage power dissipation in FPGAs and present a "no cost" approach for active leakage reduction. It is well-known that the leakage power consumed by a digital CMOS circuit depends strongly on the state of its inputs. Our leakage reduction technique leverages a fundamental property of basic FPGA logic elements (look-up-tables) that allows a logic signal in an FPGA design to be interchanged with its complemented form without any area or delay penalty. We apply this property to ...

Keywords: FPGAs, field-programmable gate arrays, leakage, low-power design, optimization, power

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next